Casio PB-2000C DL-Pascal 1.2 Installation
Motherboard ROM Swap & Gate Array Modifications

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Introduction

This document details the hardware modifications required to solder a DL-Pascal 1.2 ROM image directly onto the PB-2000C mainboard, bypassing the standard setup that relies on a removable ROM card inserted into the expansion slot.

History

Developed around 1989 by the Swedish firm Data-Larsson, DL-Pascal was a remarkable product that brought a fully functional Pascal environment—complete with an editor, compiler, and debugger—to the CASIO PB-2000C pocket computer.

Unlike the standard interpreted languages available for this platform, DL-Pascal was a true compiler generating native machine code for the Hitachi HD61700 architecture. It also introduced useful workflow features, including batch file execution for script automation and native support for the MD-100 floppy disk drive (utilizing its 320 kB 3.5" disks for expanded file and program storage). Image showing a pristine DL-Pascal 1.2 ROM Language Card.

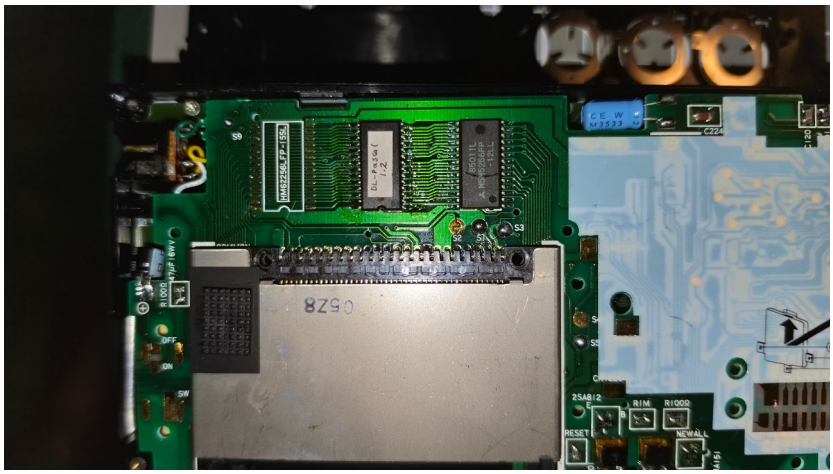


DL-Pascal initially existed as a scarce pre-release build (version 0C), with perhaps only one or two physical ROM cards surviving today. It was succeeded by version 1.2, the software's single production release. Despite its brief commercial lifespan and lack of subsequent versions, this remarkable piece of computing history endured thanks to a small community of vintage preservationists who kept it alive.

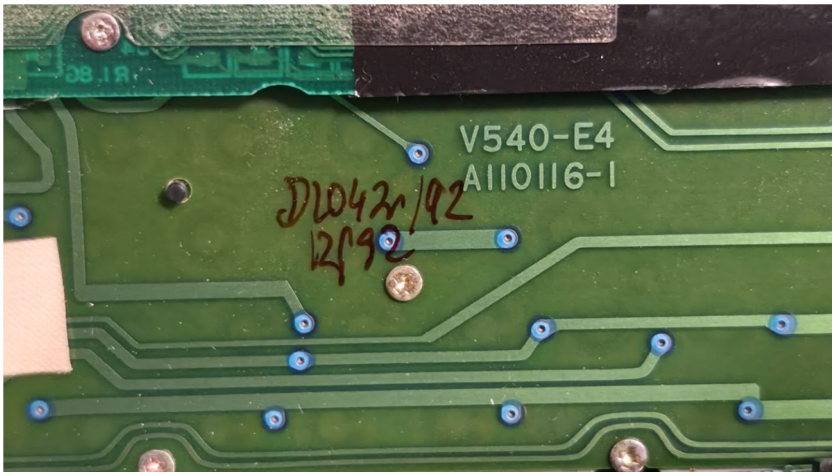
DL-Pascal 1.2 saw a remarkably small production run consisting of approximately 70 expansion ROM cards and 50 mainboard-modified PB-2000C units (Source Silicium). It was quietly withdrawn from the market without a clear explanation, only adding to the mystique of its short-lived commercial existence.

Rick Schwartz[1] documents a very rare mainboard-modified PB-2000C.

Note the handwritten label on the ROM next to the empty memory expansion slot, probably by Hans Larsson himself.



A remarkable picture in Rick's album hints at the provenance of this particular PB-2000C. Sequence 42, December 1992.



1 Visit his PB-2000C photo album, a treasure trove, kindly shared here.

Signal Names

The ROM0..ROM3 nomenclature used in this document corresponds to the following signal names listed on p. 5 of the Service Manual:

ROM0	RCE, Chip select signal to ROM (uPD27C512G).
ROM1	RA1M, No connection.
ROM2, ROM3	CCE1, CCE2, Chip select signal to ROM card.

ROM Images

According to Silicium's user Xerxes, there are four known ROM image variants: version 0.9 tested on a Sharp PC-E500, version 0C pre-release for the PB-2000C, the official release version 1.2 for standard expansion cards (selected via ROM2), and the internal version 1.2 engineered for mainboard-soldered configurations (selected via ROM0 and ROM3).

Unlike other ROM images of the period available on the Internet Archive, DL-Pascal images remain in private hands, existing only in the form of physical cards, modified PB-2000Cs and carefully guarded ROM images.

The ROM images of the official CASIO Language Cards (C, Lisp, Prolog, BASIC, CASL) do not require modification to operate either as card images or soldered ROM images. They are mapped to bank 0 and selected by ROM0 or ROM2. This is due to the fact that they do not use addresses below 0x0C12.

DL-Pascal 1.2 uses all 64 kB, so it can not be used solely in bank 0.
The lower half should also be mapped to bank 3. In the case of the soldered version, this is not possible without the hardware modification described later in this document.

ROM Differences

We deeply respect the original copyright's owner, Hans Larsson, and will only describe the differences needed to modify an original DL-Pascal 1.2 ROM card image to operate in the ROM0-ROM3 configuration.

Offset: 0x0D81 | Modified: 0x95
Offset: 0x0D82 | Modified: 0x0D
Offset: 0x0D95 | Modified: 0xD1
Offset: 0x0D96 | Modified: 0x00
Offset: 0x0D97 | Modified: 0x00
Offset: 0x0D98 | Modified: 0x43
Offset: 0x0D99 | Modified: 0xD1
Offset: 0x0D9A | Modified: 0x02
Offset: 0x0D9B | Modified: 0x1B
Offset: 0x0D9C | Modified: 0x40
Offset: 0x0D9D | Modified: 0x37
Offset: 0x0D9E | Modified: 0x1C
Offset: 0x0D9F | Modified: 0x00
Offset: 0x43F1 | Modified: 0xC0
Offset: 0x43F2 | Modified: 0x03
Offset: 0x4422 | Modified: 0x00
Offset: 0x4423 | Modified: 0x43

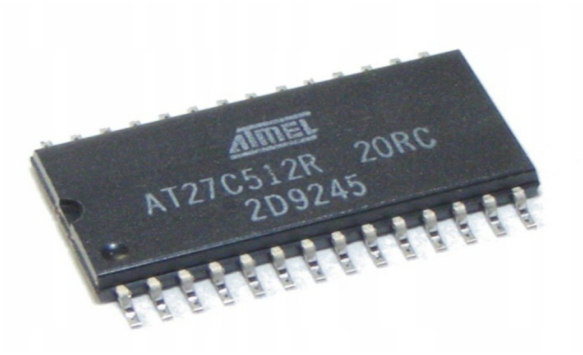
We used Piotr Piatek's PB-2000C emulator to prepare and verify the ROM image.

Step	Description
1	Create a new directory with all the extracted emulator's files.
2	Copy an original card owner's ROM dump of DL-Pascal 1.2 into rom2.bin.
3	Verify that this is a working copy by running the emulator.
4	Copy the rom2.bin file to rom1.bin and modify it per the instructions. The sha256sum of the modified rom1.bin file should be: 87e0152c52d63ba28ff95f8847953577731ef6383ad5fb640688402a4a45e5b6
5	Remove rom2.bin.
6	Copy rom1.bin to rom3.bin.
7	Verify that this configuration is working by running the emulator

It is possible to follow a different workflow—for example, if you prepared the rom2.bin file on another platform. Regardless of the workflow used, the emulator directory must contain rom1.bin and rom3.bin, **both containing identical copies of the modified ROM image**, and must not contain a rom2.bin file.

PROM Selection

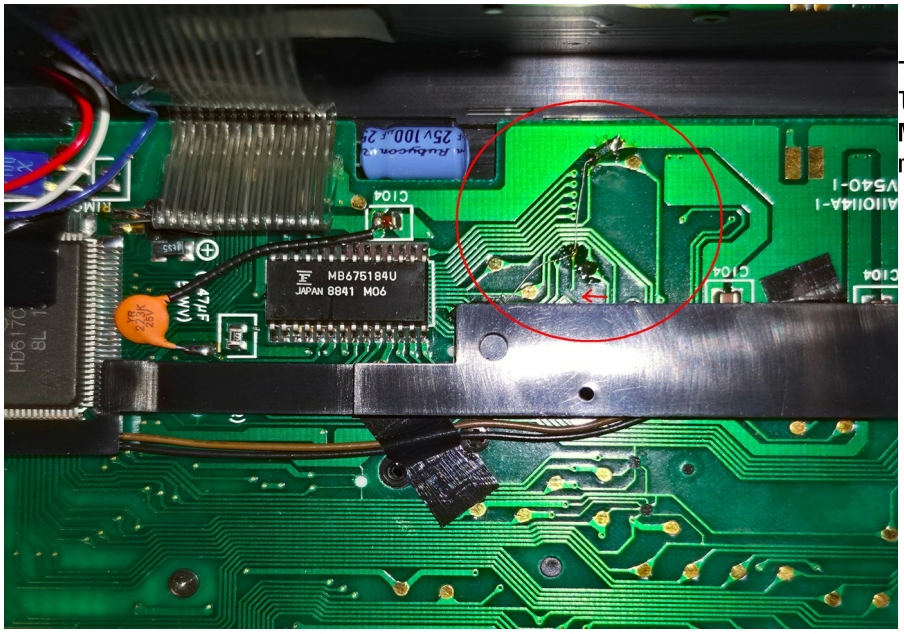
We recently achieved good results using an M27V512-120N1 (a 28F512-compatible, OTP EPROM) in a Casio ROM language card replica project. Although this IC is rated for 3.3V, its early 3.3V architecture—designed during the industry transition from 5.0V—allows it to operate reliably in this application.



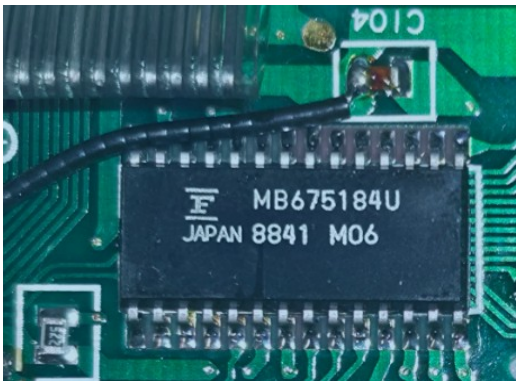
Another alternative is 27C512, OTP memory EPROM AT27C512R-20RC 512Kb SO-28 from Atmel.

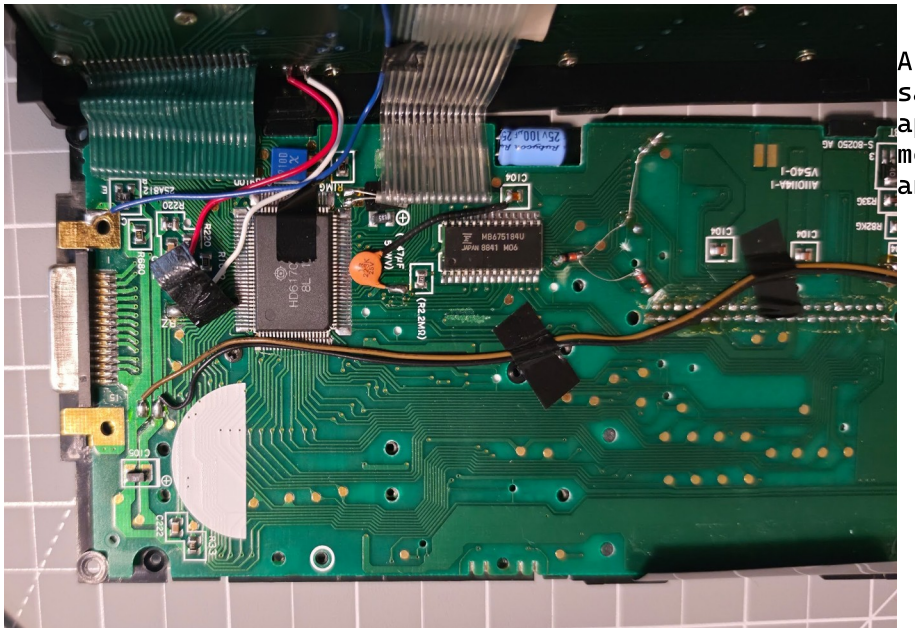
NOTE: This is the incorrect package form. Left here to document that even our best efforts sometimes are not enough. The package is SOP and the tested IC model was AT27C512R-20RC.

Hardware Modifications



The left picture shows the leads into the Gate Array **MB675184U** (right) in a modified PB-2000C.

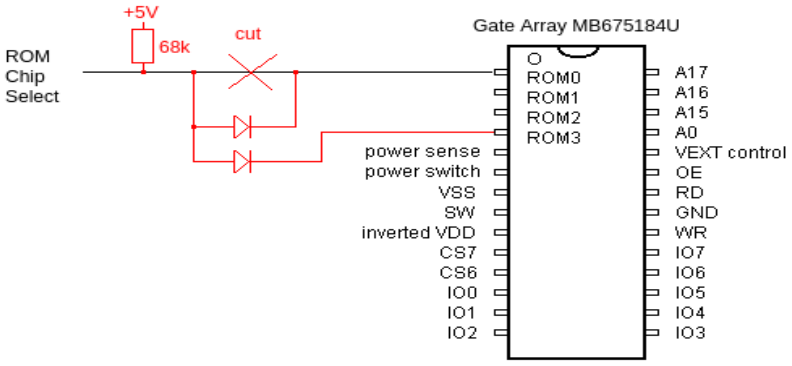


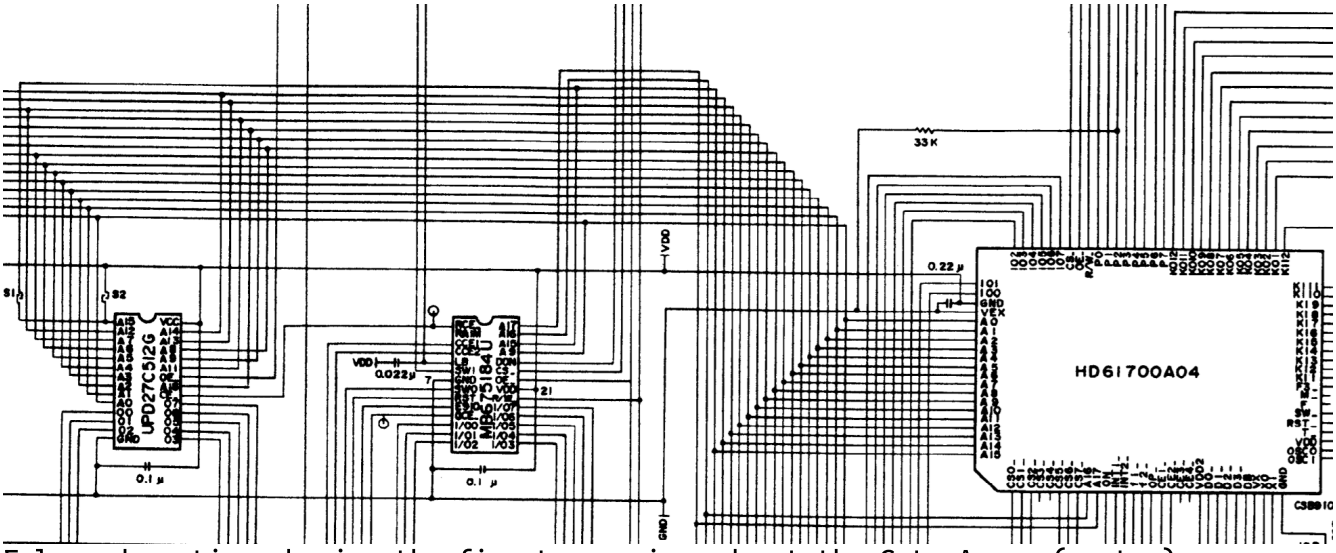


A clearer picture of the same modified PB-2000C apparently showing trace modifications, a resistor and two diodes.

Piotr inferred the following schematic for the modification.

A pull-up resistor, two diodes.





Enlarged section showing the fine traces in and out the Gate Array (center).

Important remarks from Piotr:

“The diodes and resistor form a poor-man's AND gate that isn't as good as a CMOS chip 74HC1G08, especially in terms of rising-edge propagation time. It may reliably work at a clock frequency of 910 kHz, but perhaps not at 2 MHz.”

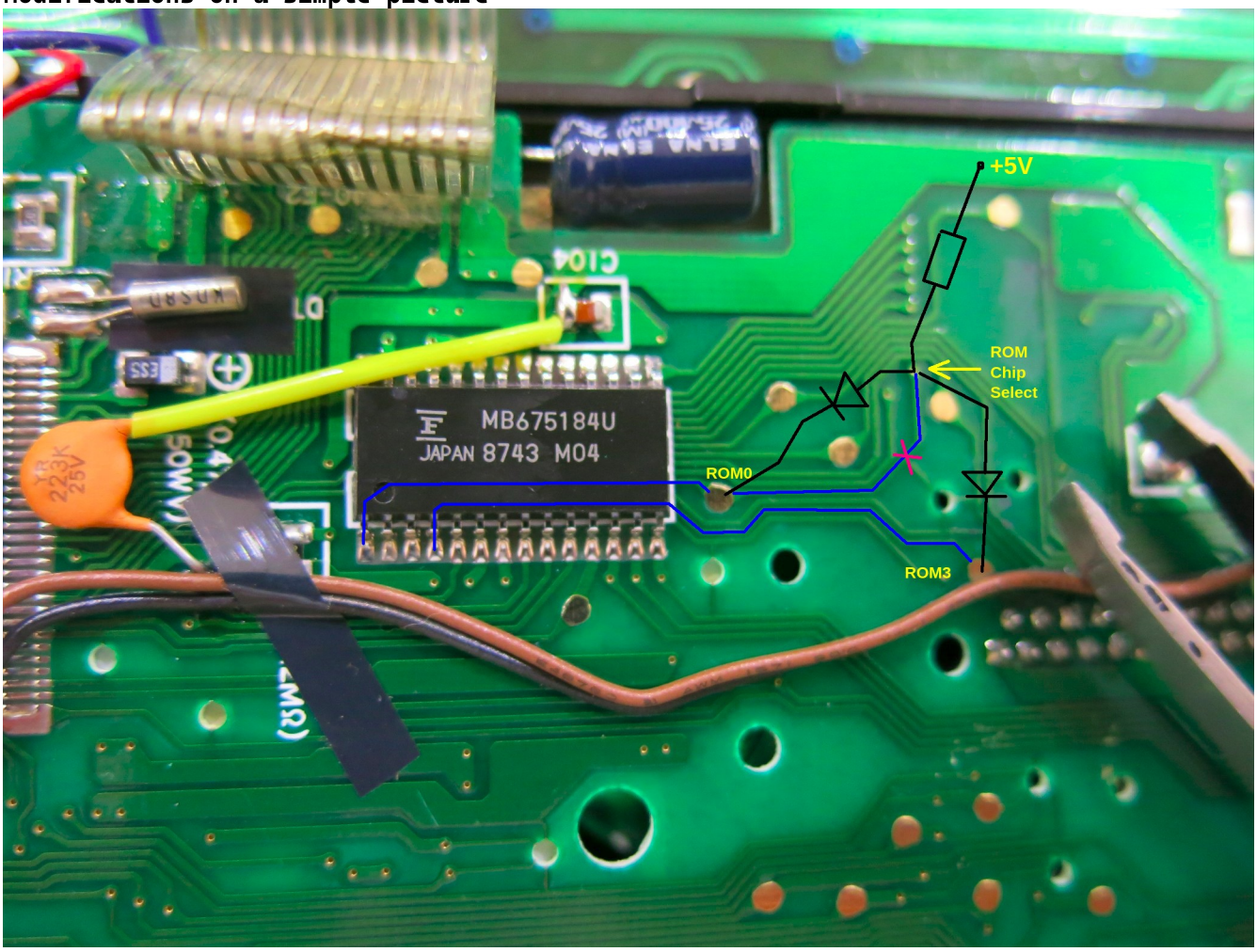
Piotr refers to the overclocking modification that replaces the standard 910 kHz oscillator with a 2 MHz one, along with the following important advisory:

“I would halve it to **33k** in advance. This would improve the voltage slew rate at the cost of insignificantly higher power consumption. “

Designed to support a future overclocking modification, with expected stable operation.

And so it shalt be done. The pull-up resistor for this modification will be 33 kΩ.

Modifications on a simple picture



And a few words from Piotr:

“I think the modifications should be performed as shown in the attached image. The relevant traces are marked blue. The red cross marks the place where the trace should be cut. I would use ordinary through-hole components instead of SMD, unless there's not enough place. I would use Schottky diodes because of lower voltage drop, but ordinary ones should work too.“

Bench-top warnings

While the modification design itself is straightforward, execution carries standard vintage hardware risks:

- **Familiarize yourself with this document, the location of the Gate Array, traces to modify and location and position of the existing ROM.**
- **Preservation:** You will replace an original CASIO mask ROM containing the c language with an OTP EPROM containing the ROM version of the DL-Pascal 1.2 image. The original CASIO ROM should be preserved and re-used in a specially labeled OM-64R card.
- **Preparation**: Take one high resolution photograph of the field to modify, and a dry-run the modifications. There should be no surprises during the execution of the modifications.
- **Document:** Document your steps as you work toward the Gate Array. Photographs, notes, and silkscreen annotations will make it much easier to reassemble the PB-2000C correctly. These notes will be invaluable to other community member willing to perform a similar modification.
- **Trace Cutting Precision:** The trace on the PCB leading to the ROM0 pin is thin. Cutting it requires a steady hand with a sharp craft knife. You must ensure you don't nick adjacent traces on the dense PB-2000C mainboard.
- **PCB & Trace Heat Sensitivity:** The PB-2000C mainboard uses vintage 1980s substrate that easily delaminates or lifts traces under excessive heat. When soldering the diode leads and resistor to the scraped traces and vias, use a temperature-controlled iron set to **300**℃ **- 320**℃ with minimal dwell time (under 2-3 seconds per joint). Avoid heating the scraped copper traces directly for too long to prevent tearing them off the board.
- **Short Circuits / Clearance:** Because space inside the PB-2000C shell is tight, ensure the diode bodies and the 33 kΩ resistor leads are insulated (using fine heat-shrink tubing or Kapton tape) so they don't short against the shielding or case when closed.

Note on the MB675184U Gate Array:

The modification instructions do not require direct interaction with the MB675184U, but it is worth documenting for community knowledge: this chip is a factory-configured logic array tailored specifically to Casio's internal hardware. Because its internal logic is proprietary, a functional replacement cannot be bought off the shelf unprogrammed—it must come directly from a PB-2000C donor board.

How to make the new ROM?

Once you have generated the new ROM image file, burn it to the OTP EPROM using one of two methods:

- **Standard Method:** Use a chip programmer with the appropriate EPROM adapter.
- **Alternative Method:** Write the image using an unprogrammed OM-64R card and its programmer adapter. Next, carefully extract the newly programmed ROM and install it into the host PB-2000C. Finally, install the original C-ROM you removed into the newly freed slot on the OM-64R card.

Bill of Materials

Item	Qty	Comments
M27V512-120N1	1	Programmed with the ROM DL-Pascal 1.2 image
33 kΩ resistor	1	Use ordinary through-hole components instead of SMD, unless there's not enough place
Schottky diodes (BAT42)	2	Use ordinary through-hole components instead of SMD, unless there's not enough place. Be sure to double-check the diode orientation before soldering

Diode Selection Note:
The original modification uses standard **1N4148** silicon switching diodes in DO-35 glass packages. While functional at the stock 910 kHz clock, builders should substitute small-signal Schottky diodes such as the **1N5711**, **BAT42**, or **BAT43**. The lower forward voltage drop of Schottky diodes ≈ 0.2V – 0.3V versus ≈ 0.7V on a 1N4148 improves logic-level margins on the EPROM Chip Select line, reducing risks of read instability under low battery voltages or higher clock frequencies

DL-Pascal 1.2 Boot Screen

After completing the modifications and closing the PB-2000C, turn it on.
Make sure that the ROM card is empty and in the lock position.

You will likely see the “New ROM card:” message (this is a very good sign):



Press [EXE]
Press [MENU] To see the initial DL-Pascal 1.2 screen:



These images were generated by the emulator running the modified ROM in the ROM3 configuration (CCE2).

Other modifications

Having established that the PB-2000C is functional with its new ROM, you can proceed with additional modifications:

- Installation of 32 kB on the motherboard. Documented here.
- Overclocking to 2 MHZ. Documented here.

If you plan to apply all three available modifications to your device, we suggest performing them in the following sequence:

1. Installation of 32 kB on the motherboard.
2. Overclocking to 2 MHZ.
3. Gate Array Modification and DL-Pascal 1.2R (motherboard ROM) installation.

Motivation

The drive to document and preserve this gate array modification stems from a desire to safeguard an innovative piece of hardware history and make its eventual reproduction possible. This hand-crafted rework represents a unique moment in late-1980s engineering. Capturing the schematic detail, trace cut, and discrete component placement ensures that this piece of technical heritage is not lost to time, giving future vintage-computing enthusiasts a clear blueprint to faithfully recreate this device.

Preservation is particularly urgent because, unlike the durable mask ROMs found on original CASIO cards, the original modification relies on EPROMs whose data will inevitably degrade. The trapped charges keeping those bits programmed are not permanent, and it is only a matter of time before charge loss causes memory cells to fail. While the lower density and more forgiving manufacturing tolerances of 1990s offer some resilience against decay, environmental factors and time will ultimately dictate their lifespan. Making logic failures around the device's 50th anniversary a distinct possibility. Securing clean ROM dumps and maintaining a comprehensive guide to applying these hardware mods are precisely what vintage electronics preservation is all about.

AI Collaboration

Portions of this document were refined in collaboration with Google’s Gemini. All errors are human.

Let me include here a verbatim comment by Gemini, produced just by looking at selected pictures and asking focused questions. Remarkable.

Gate Array Patch / Mod

- **Components:** The patch near the Fujitsu gate array (**MB675184U**) includes the dead-bug wired **pull-up resistor (68k)** and two **diodes** (1N4148 style) soldered directly onto scraped traces and nearby vias.
- **Trace Scrapes:** Multiple traces on the green mask have been severed or scraped back to tap directly into specific signal lines feeding into the gate array logic.
- **Execution:** A classic hand-crafted prototype fix or hardware patch—functional, but definitely done freehand on the bench.

Later, Piotr recommended 33k for the pull-up resistor, but the AI interpretation was accurate.

Field Experience: Wrong packaging

It happens.

Daniel Falcon, our tech, opened the test PB-2000C and calmly said, “the ROM on the motherboard is not TSOP-28 it is SOP-28.” Oh well, M27V512-120N1, our initial design is incorrect-N stands for TSOP. He then decided to purchase the AT27C512R-20RC. For Atmel, the R stands for Small Outline Integrated Circuit package, which is commonly referred to as an SOP. Also attractive for its 200 ns period correct access time. Live and learn. The M27V512-120N1 is an old friend and we **all** got confused.

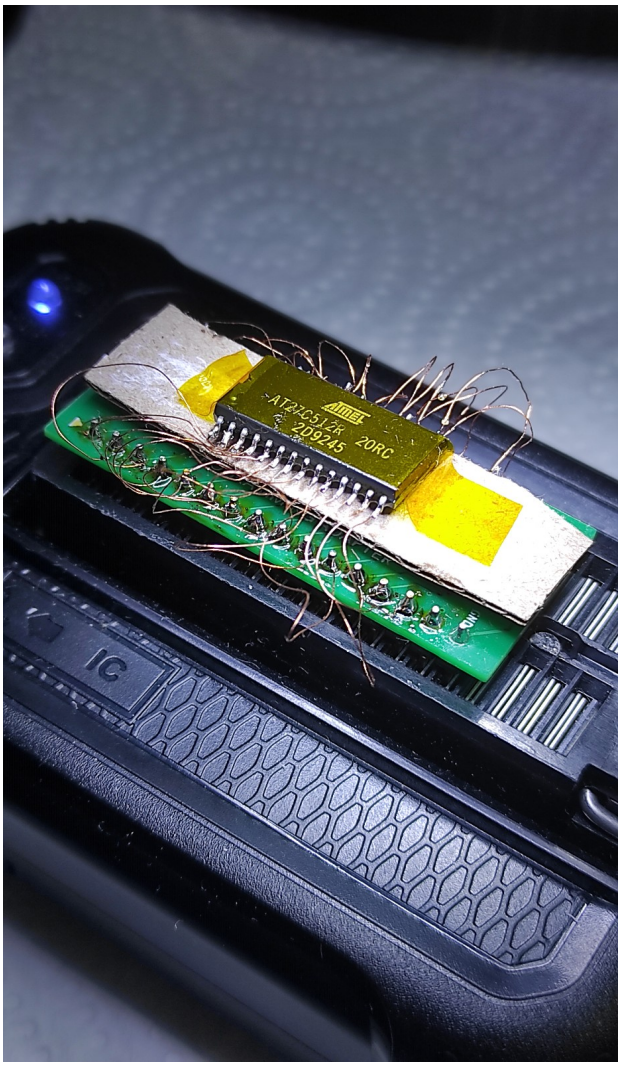
First Success Report

Pictures are worth a thousand words.



No adapter? No problem.





Acknowledgments

This User Guide was produced by Xandrian Labs. 付喪神.

Special thanks to Betka for her continued and loyal support.

This is a collaboration with Gemini. All errors are human.

This work is freely shared with the vintage computing community. Please use it, build upon it, and cite the source.

Final.